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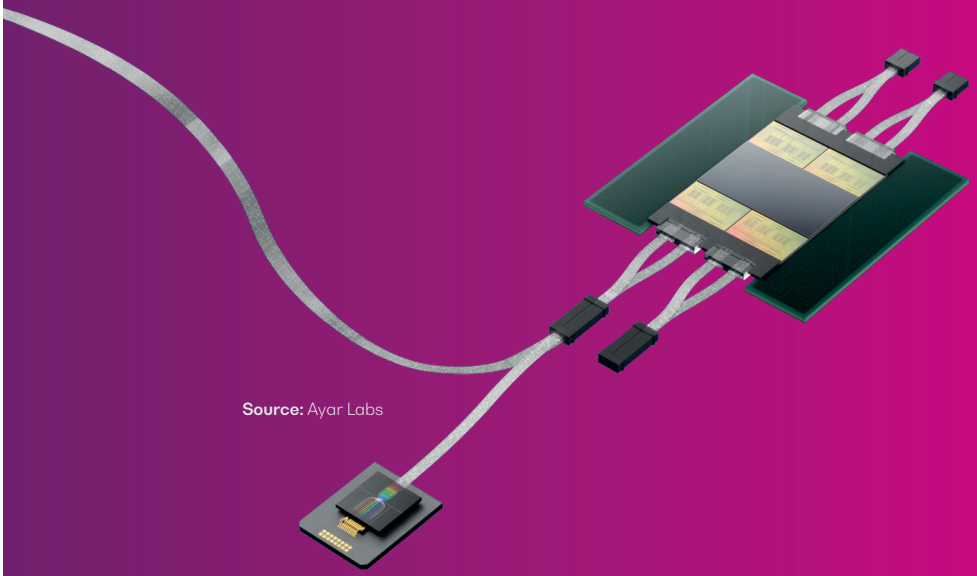
Testing Strategies for Next-Generation Optical Interconnects: Co-Packaged Optics & Integrated Photonics

WHITE PAPER

This paper discusses industry trends in Integrated Photonics and how market participants are adapting to test and mass produce next-generation optical interconnects in a cost-effective manner. The traditional semi-conductor ecosystem is the example for the industry and parallels can be made with the current evolution of the Integrated Photonics ecosystem.

By **Kees Propstra**



Source: Ayar Labs

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Introduction

The world of optical interconnects is changing rapidly, and test solutions need to evolve to address emerging needs. There are three key trends making a significant impact on the optical interconnect ecosystem. But first, we must consider two trends that are driving change in the interconnect ecosystem.

Image 1: Data center.

First, there is insatiable demand for bandwidth. Technology is interweaved with our personal and professional lives and 5G networks are providing internet access everywhere and all of the time. At the bottom of this 'food chain' are the data centers and computer networks with typical equipment such as servers, switches, and storage devices and high-performance compute platforms. This is where data is stored and routed anywhere in the world at the flick of a switch. Complex algorithms are required to keep data flowing smoothly and seamlessly, while fast-growing applications such as machine learning and artificial intelligence place even more demand on the system.

Second, the overwhelming majority of these devices are currently interconnected with 100 Gbps per channel via optical interconnects, because traditional copper interconnects can maintain 100 Gbps over only a few meters.

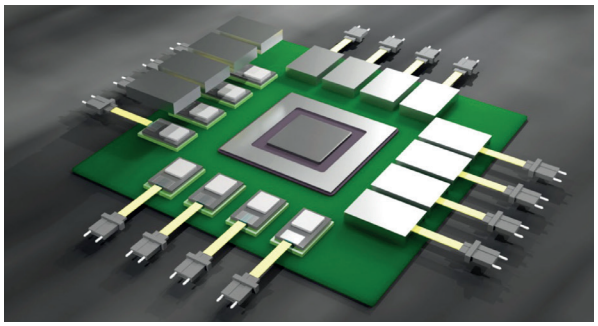
The three key trends making a significant mark on the industry are:

1. Photonic Integrated Circuits (PICs)

Current integrated photonic approaches utilize Silicon Photonics and similar technologies to combine multiple electro-optical functions into a single photonic integrated circuit (PIC). These functions would normally be provided by multiple, separate optical components, such as modulators, wavelength (de)multiplexers and detectors. The dense integration of components reduces footprint and power consumption, and ultimately improves the cost structure of optical interconnects. This approach also enables the provision of more bandwidth per front panel, paving the way for 50 and 100 Tbps single-height switch racks[1].

Image 2: Photonic IC.

2. Co-Packaged Optics (CPO)



Since power consumption is one of the most important concerns for next-generation data centers, (in addition to bandwidth, size and cost), there is a trend to bring the optics and switch ASIC as close as possible, and even integrate them onto the same substrate or into the same package to avoid or minimize lossy PCB traces[2].

Image 3: Broadcom's 51.2T CPO drives 30% power, 40% cost and 50% density improvement compared to traditional pluggables. (**Source:** Broadcom).

Although there may not yet be exact agreement on what this is going to look like, there is consensus in the industry that this concept of bringing the optics close to the electrical IC has merit and there are lots of ongoing activities to make this a reality. A good example is the OIF 3.2T Co-Packaged Optical Module Working Group which is driving standardization around this concept[3].

3. Disaggregated Networks

Lastly is the notion that current high-performance computer architectures have bottlenecks that can be resolved by disaggregating typical computer functions such as processors, memory, accelerators, and storage, to optimize the computational efficiency and connecting them with standardized, low-latency, high-bandwidth optical interconnects[4].

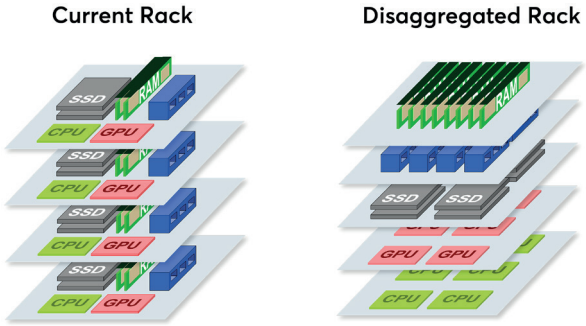


Image 4: Standard versus disaggregated rack. (**Source:** Ayar Labs).

Machine Learning and Artificial Intelligence will rely heavily on next-generation compute platforms, therefore addressing these bottlenecks should be an immediate priority of the interconnect technology evolution. Ayar Labs is pioneering their in-package optical I/O solution, combining their TeraPHY™ optical I/O chiplet and SuperNova™ external light source, to address this performance bottleneck and enable the build-out of massive high-performance computer networks at reduced cost and power consumption.

The combination of PICs, CPO and disaggregation is driving the development of very densely packed, high-channel-count optical modules with hundreds of channels that enable the 50T and 100T network switches as well as the next generation of supercomputer networks (1000+ petaFlops). These trends have a major impact on the testing ecosystem that will be discussed in this paper. For more details on co-packaged devices, an overview can be found in the COBO 'Design Considerations of Optical Connectivity in a Co-Packaged or On-Board Optics Switch' white paper[5].

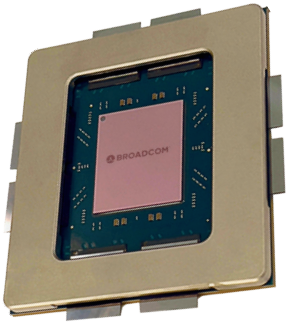


Image 5: A Broadcom Co-Packaged Optical device (**Source:** Broadcom).

Test Challenges

Production Stages - PIC

Modern wafer-based technologies such as Silicon Photonics and Photonic Integrated Circuits typically require three levels of testing: wafer, die/assembly, and packaged product. The more traditional discrete optical technologies have a comparable breakdown of testing needs, which starts at the component level, to optical subassembly, and packaged product.

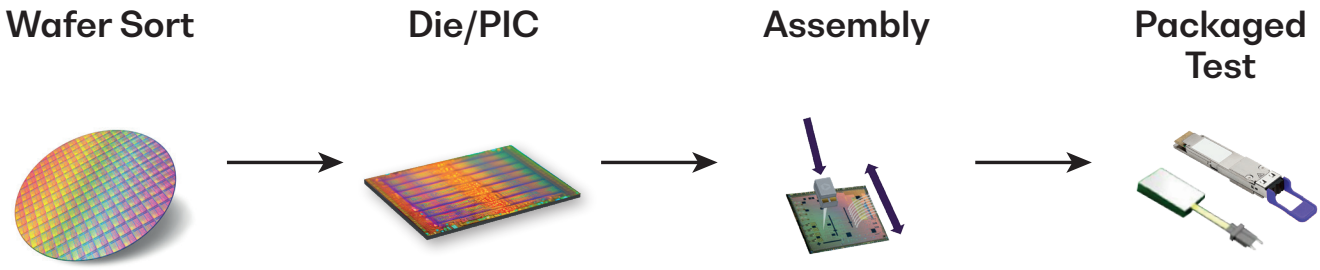


Figure 1: Production and testing stages for silicon photonics and PIC manufacturing.

The first step comprises a wafer sort, where a few tests need to be conducted to determine whether the functional PICs on the wafer have sufficient quality to proceed to the next step. For this first step a probing system is required to inject and extract light from the optical structure as well as electrical probe cards to power any active components, in combination with a wafer handling system. In general, this is the most cost-effective test stage to identify manufacturing defects, and there are tangible benefits to increasing test coverage at this stage.

Once the wafer has passed the initial tests, it will be diced into smaller sections with singular or multiple dies. Now another test will determine whether each individual die meets the requirements to be assembled into the final product. Similarly, to the first step, complex handling and probing equipment is needed to process the die.

After the die has passed this stage the final assembly and alignment will take place. In some cases, additional components or chiplets will be added to the die in yet another manufacturing step. These 2.5D integrated optical sub-assemblies will require some testing prior to moving to the next manufacturing stage. Again, the assembly and alignment equipment has to function in perfect harmony with the test equipment. A common consideration of the test engineer is the trade-off between time and resources necessary for testing early and frequently, and devices failing T&M later in the production process. As the cost of failure increases along the production process, inappropriate T&M can reduce the cost-effectiveness of the process, which translates into a higher unit cost for the final useable products.

Therefore, it is crucial to enable optical testing throughout the stages of the PIC product life cycle. Test equipment must work in concert with auxiliary equipment such as wafer handlers, probing stations, assembly and alignment equipment, as well as fully packaged device handlers.

Photonics Tests

What is actually tested depends heavily on the DUT, but in the case of Integrated Photonics for data communication, the following examples are fairly standard. In addition, some examples of typical tests setups will be provided in the section of photonics testing.

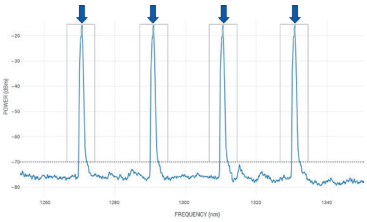


Image 6: CWDM Demux filter wavelength test.

Passive tests

These tests range from insertion loss and return loss of the waveguide structure, including polarization and wavelength dependence as a figure of merit of the DUT. For example, a full parametric characterization of a wavelength demultiplexing filter falls under this category.

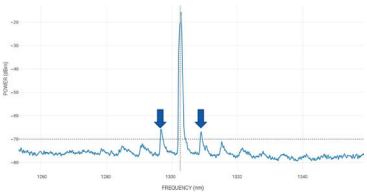


Image 7: Laser SMSR (side mode suppression ratio) test.

Active tests

In this case the optical performance such as modulation depth or wavelength sensitivity are tested as a function of a relatively low-speed control signal. A validation of the optical spectrum of an active device falls also under this category.

Image 8: Bit-error-ratio (BER) test.

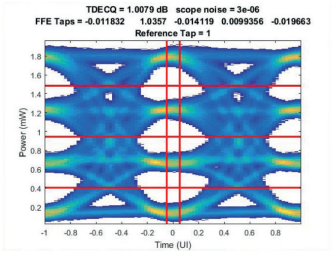


Image 9: Eye Diagram TDECQ measurement.

At-speed tests

A special category of active test is the full at-speed characterization of the device using internal or external high-speed data generators to enable eye diagram measurements or bit error rate measurements. Compliance testing typically falls under this category, where standards organizations such as OIF and IEEE define test requirements that fully characterize the device technology at the product level.

Image 10: Environmental test chamber.

Environmental stress testing/HALT

Another test category that is especially critical for Photonics products, such as optical transceiver modules including CPO technology, is environmental stress testing and highly accelerated life testing (HALT). This category focuses on the proper operation over the intended operating conditions as well as longevity of the product and tests exposure to high humidity and temperature to demonstrate that these products are reliable and have an acceptable mean-time-between-failure (MTBF). Next-generation optical modules will carry 1.6 and 3.2 Tbps of data transfer and are an important link in the overall communication chain therefore this pre-emptive focus on reliability.

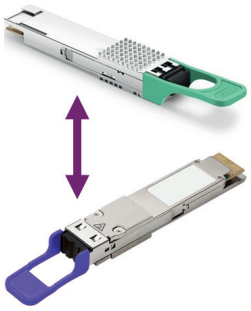


Image 11: Interop testing between transceivers.

Interoperability

Testing the transmitter and receiver characteristics in the previous categories is important but may not reveal all the issues once plugged into a real system. Therefore, system and link testing between different vendors' optics in a real life network environment is an important test category as well. The latter two test categories are important but will not be discussed in detail in this paper.

Product Life Cycle

In addition to the manufacturing stages, testing requirements can be broken down to the phase in the product life cycle; from R&D, validation/characterization, and volume manufacturing. Deployment is another phase in which the test requirements differ from the previous phases. In the **R&D phase**, versatile test equipment is required to debug early designs and validate design principles. High-precision instrumentation is key to understanding true device performance, and wide test coverage is important to understand design trade-offs. This testing is executed by very capable expert-level engineers and would be very hands-on.

The **validation or characterization phase** involves the full, multi-corner performance characterization of the design. Multiple products will be tested across all operating conditions and process/design corners as part of a complete Design Verification Test (DVT).

Accuracy and broad measurement support are critical to ensure the true device characterization with full understanding of the observed results. This mostly automated testing phase is overseen by the experienced test engineering teams, and will inform which parameters must be tested during volume manufacturing to ensure product performance.

Volume manufacturing testing is designed to be a quick optimization routine and cost-effective screen to guarantee that only specification-compliant products are shipped to end users. There is some flexibility to select the pass/fail criteria, and this relies heavily on the data collection in the previous phase. Cost-of-test, test time and correlation to established measurement standards are critical criteria for this phase. Specialized manufacturing test engineering teams manage this as part of the product life cycle.

Once technologies have matured and products are shipping and ready to be deployed in live systems, there is a new range of testing required. Rapid testing to check a product meets the expected requirements as part of the RMA process or **incoming inspection.** System tests with all products installed, or interop testing between different suppliers are all counted in this testing category. The former tests should be done in a technician- or operator-friendly environment, which will benefit from a fully automated, single push button test solution. The latter-interop testing - requires management of complex testing routines and typically falls under engineering's responsibility.

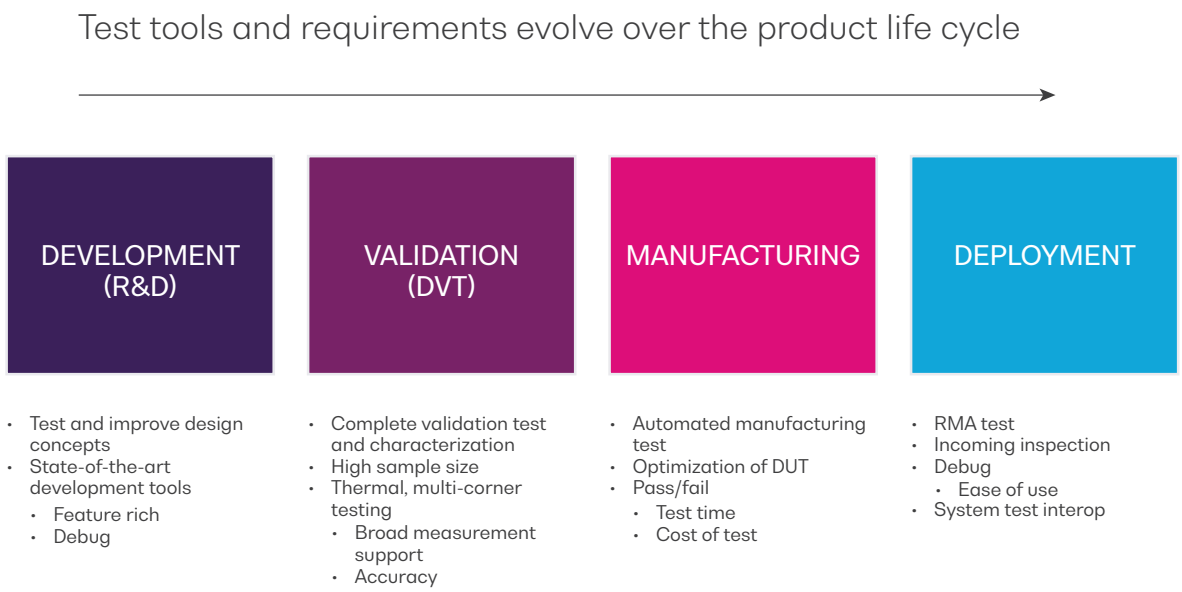


Figure 2: Tools and requirements change as products enter new phases of the life-cycle.

The traditional electronic semiconductor ecosystem is often the reference point for the Photonics IC industry as electronic semiconductor testing has matured over five decades and is able to produce billions of high-quality products every year. The fabless business model with test and assembly partners, as well as contract manufacturers works extremely well, and is the envy of the Photonics IC industry[6].

The next few years will require a concerted effort from all ecosystem participants to retool the test and assembly houses (OSATs) and contract manufacturers (CMs) and add the optical test and assembly capabilities to be able to produce quality Photonic ICs and high-density, high-channel-count optical modules in significant volumes and make it commercially attractive. More information about what the dense integration of photonics means for testing can be found in our Testing Considerations for High-Density Co-Packaged Optical Devices – White Paper[7].

Photonic IC Ecosystem

The application, end-user side of the Photonics IC ecosystem, starts with the developers of the photonics technology and components at the bottom of the food chain. Here, the photonics component technology or optical subassemblies will be integrated into optical modules in combination with the typical SerDes electrical technology. The optical modules go either directly to the system integrators or pass through a value-added reseller, or third party optics supplier for further optimization.

System integrators combine the optics with the switches and servers, and add sophisticated system software to create the Ethernet network equipment and systems. In the final step, at the top of the food chain, the hyperscale data center and/or internet service provider combines all this equipment into the mega-platforms on which the internetworking services are being offered.

As previously mentioned, the optical interconnect technology is a hard requirement due to the combination of high throughput and distance which can only be achieved with optical links.

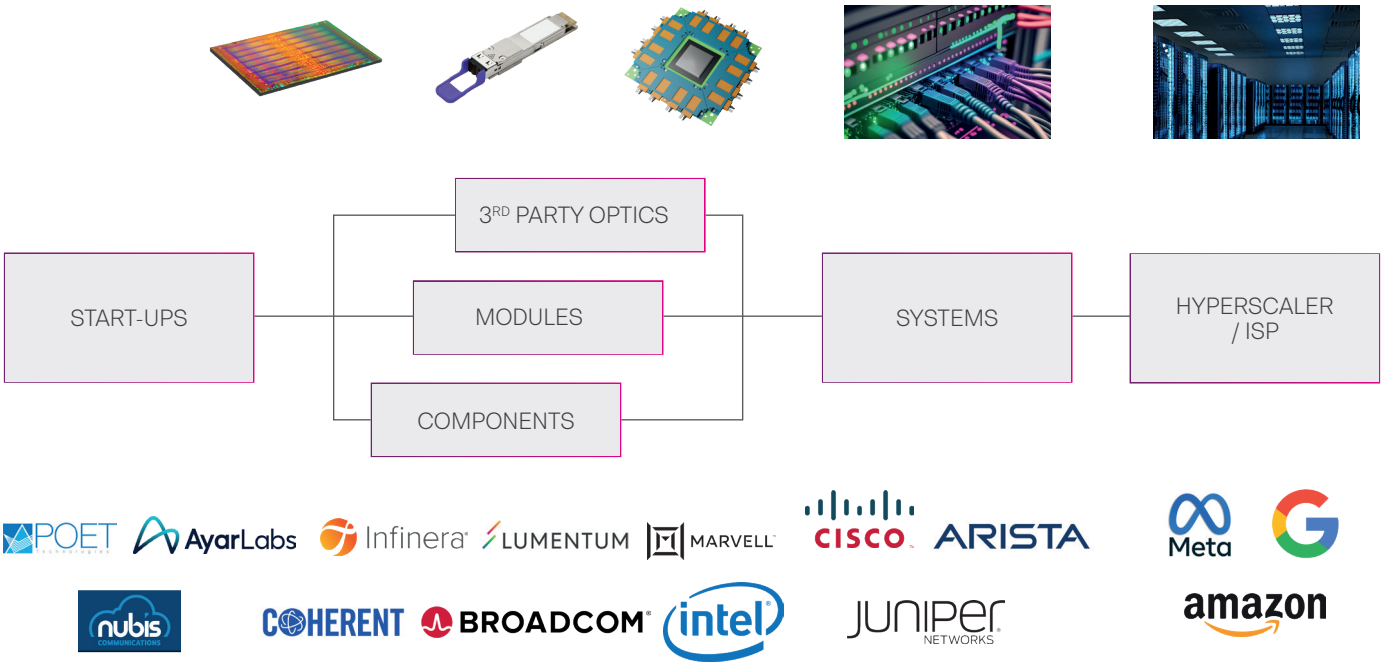


Figure 3: An overview of the main segments and companies involved in the application and end-user side of the PIC ecosystem.

The other side of the ecosystem focuses more on the design and manufacturing of the photonics products, which is of course heavily intertwined with the end-user applications. The photonic integrated circuit is designed from scratch or uses existing building blocks from an IP library. Design and layout software is used to roll the designs into the PDK and eventually produce wafers at a photonic integrated circuit wafer foundry.

The foundries manufacture wafers that need testing before being diced into smaller dies or PICs. Wafer sort testing helps the selection of the wafers and on-wafer testing aids the selection of the in-spec, functional dies. Specialized photonics

test houses, the photonics equivalent of the so-called Outsourced Semiconductor Assembly and Test (OSAT) houses, are ramping up their photonics test capabilities to be able to support this service.

Once the right dies have been selected the assembly can take place, with the optics packaged into pluggable small modules, or as part of a co-packaged optics structure. Typically, a contract manufacturer takes care of this final step.

Each of these steps rely heavily on photonics wafer handlers and assembly equipment. Consequently, optimized photonics equipment with integrated test capabilities plays a critical role in the ecosystem.

In reality the ecosystem is more complex with fabless chip companies versus integrated device manufacturers (IDMs), as well as original design manufacturers (ODMs) and original equipment manufacturers (OEMs) that play a very important role in the manufacturing and realization of these technologies. However, they will all have comparable test and measurement challenges that are being discussed in this overview paper.

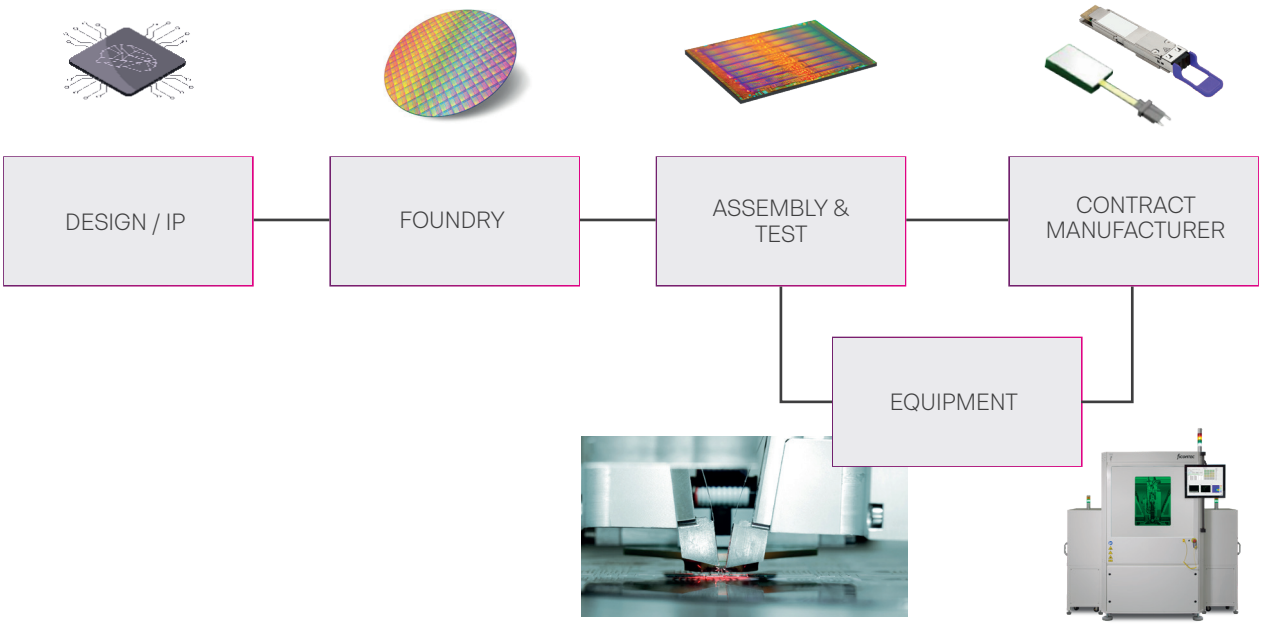


Figure 4: An overview of the main design and manufacturing stages of the PIC ecosystem.

Testing Considerations

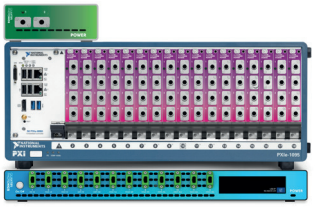
In summary, the test solutions to support the evolution in Optical Interconnects need to address the following requirements:

1. Support next-generation photonics IC testing from wafer to packaged product
2. Integration with probing, assembly and alignment equipment for optimized test flows and throughput
3. Ability to test miniaturized, high-channel-count (100+) devices cost-effectively
4. Support variable mix of test parameters to enable testing throughout the product life cycle from R&D to manufacturing and beyond
5. Enable manufacturing testing in high volumes in the most cost-effective manner

To address these requirements, Quantifi Photonics' test platform supports the following characteristics:

Flexible

Being able to choose from a wide selection of test modules in a variety of form factors, including the PXI test bench, and vary the mix as the testing needs evolve.



Scalable

Increase test system channel count from a few channels to multi-DUT, multi-port testing up to hundreds of channels simultaneously, in a cost-effective manner, ideally suited for manufacturing environments.

High-Density

The field-proven PXI test platform can support up to 17 single width test modules in a single 4 U high, 19-inch test rack. In addition, custom test configurations can be designed into an even higher density form factor to achieve the ultimate testing cost-effectiveness and density especially in a manufacturing environment.

True Mixed-Signal

Bring both optical and electrical testing together in a cohesive platform that is fully integrated to work together, enabling unparalleled testing time improvements.

Versatile

Quantifi Photonics offers a wide selection of optical and electrical test functions that can be used to build a complete optical test bench, from fixed and tunable lasers to multi-channel photodetectors, as well as bit-error-rate testers and optical-to-electrical convertors.

Ease of Integration

Quantifi Photonics instruments use a common GUI and API and can be easily integrated into a larger system with assembly equipment. With added support of the novel gRPC remote control protocol, Quantifi Photonics instruments offer an additional level of smooth and responsive system integration.

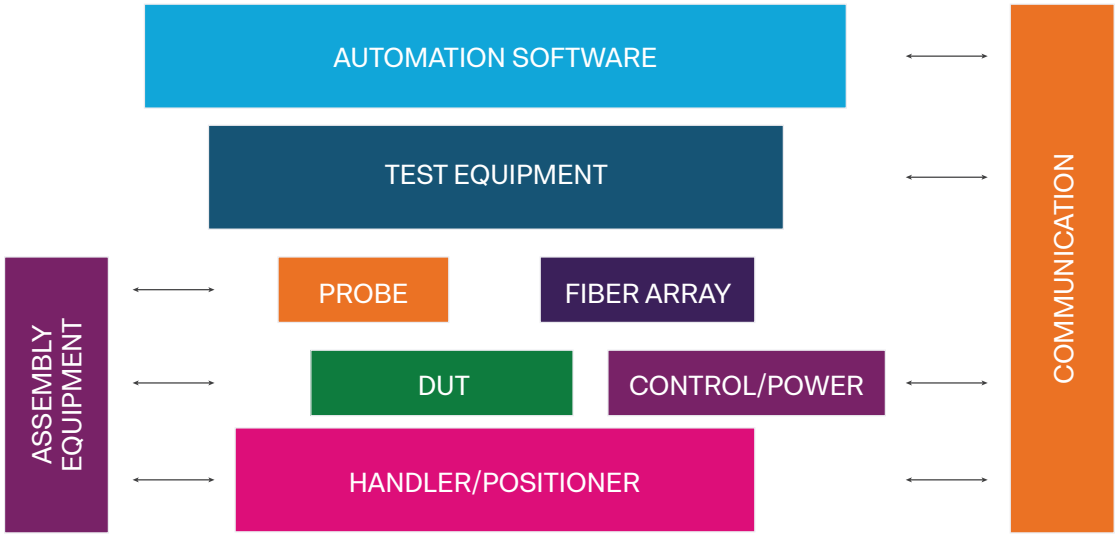


Figure 5: Photonics IC testing requires a range of specialized components, equipment and software working seamlessly to perform a range of complex test procedures.

Photonic Testing

The typical photonics test set up comprises the following elements:

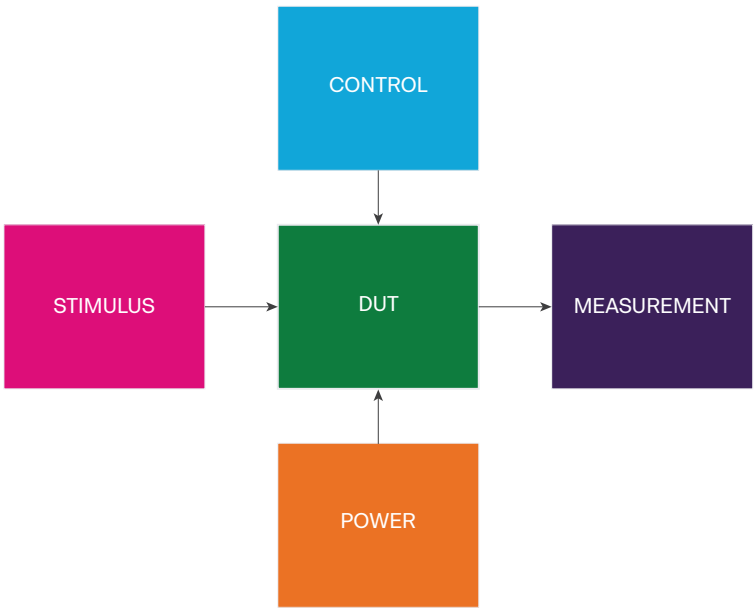


Figure 6: A simplified example of the main components of a photonics test system.

Device-Under-Test (DUT)

The DUT can be a wafer, a die, or a packaged part, with a specific optical function such as an array of ring resonators, or laser diodes, or a more complete integrated optical transceiver function. This is in addition to the more traditional optical (sub-) components or subassemblies.

Stimulus

A stimulus is required to activate the device, which can be a polarized light beam of a certain wavelength, or a swept wavelength laser to present the whole spectrum of interest. In some cases, an electrical stimulus may be required to activate the desired test mode. This can be a low-speed control signal, for instance, to measure the Vpi voltage of an optical modulator. It can also be an electrical high speed data stream as input to the optical modulator to test the at-speed responsiveness.

Control

There typically is a need to control the DUT, either to just initialize it or to step through the device settings for optimization purposes. For instance in case of the broadly adopted Common Management Interface Specification (CMIS) interface[8] a low speed I2C is chosen to accomplish this task.

Power

The device needs to be powered with the proper power supply lines to be able to operate as intended, and in addition certain bias voltages may be required for the desired operation of the signal modulators.

Measurement

On the measurement side there is a range of potential options from power levels to test waveguide quality and alignment, to the optical spectrum of lasers or wavelength multiplexers and filters, to high-speed signal eye diagram measurements such as TDECQ, AOP, ER, and jitter. In some cases, the electrical high-speed signals are measured as well as part of the bit-error-rate testing for optical receiver sensitivity testing.

Examples

The following examples illustrate use cases for Integrated Photonics testing:

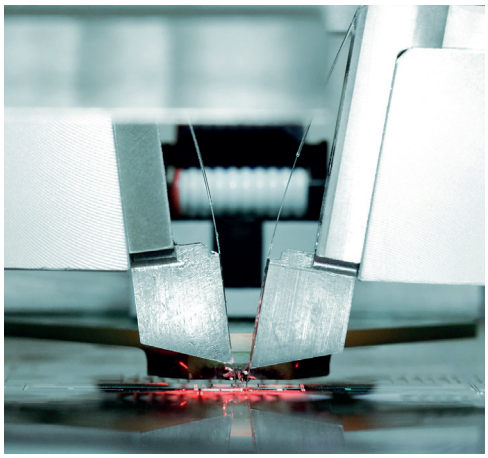


Image 12: Wafer probe system. (**Source:** ficonTEC Service GmbH).

Wafer-level inspection - wavelength and polarization dependent behavior

This example comprises a setup with wafer handler and a probing system to be able to inject the optical signal into and measure the optical signal out of the device under test. The input light consists of a swept laser to perform wavelength dependent measurements, and a polarization controller to condition the input polarization.

The setup also requires optical power monitors to measure the optical power levels as a function of the wavelength and/or polarization sweep. The setup is further augmented with optical switches to measure insertion loss and return loss in a fully automated way. In addition, variable optical attenuators can be used to control the power levels for precise sensitivity testing to complete the test coverage.

An example of a generic wafer probing and measurement set up is shown below (figure 7). Depending on the specific needs the input test equipment can range from:

- Fixed laser – provide a precisely controlled specific optical wavelength signal
- Swept laser – sweep through the wavelengths of interest
- Optical amplifier – boost the optical signal to the desired level
- Polarization conditioner – control the polarization of light accurately or sweep through all polarization states of interest (Poincaré sphere)

In addition, the test equipment monitoring the output optical signal typically varies from the following selection:

- Optical spectrum analyzer – analyze the optical power as a function of wavelength
- Optical power detector – measure the optical power to determine insertion loss or optimize alignment
- Optical to electrical converter – bring the optical signal into the electrical domain for further analysis
- Oscilloscope/clock recovery – track the high-speed optical signal and provide eye diagram analysis

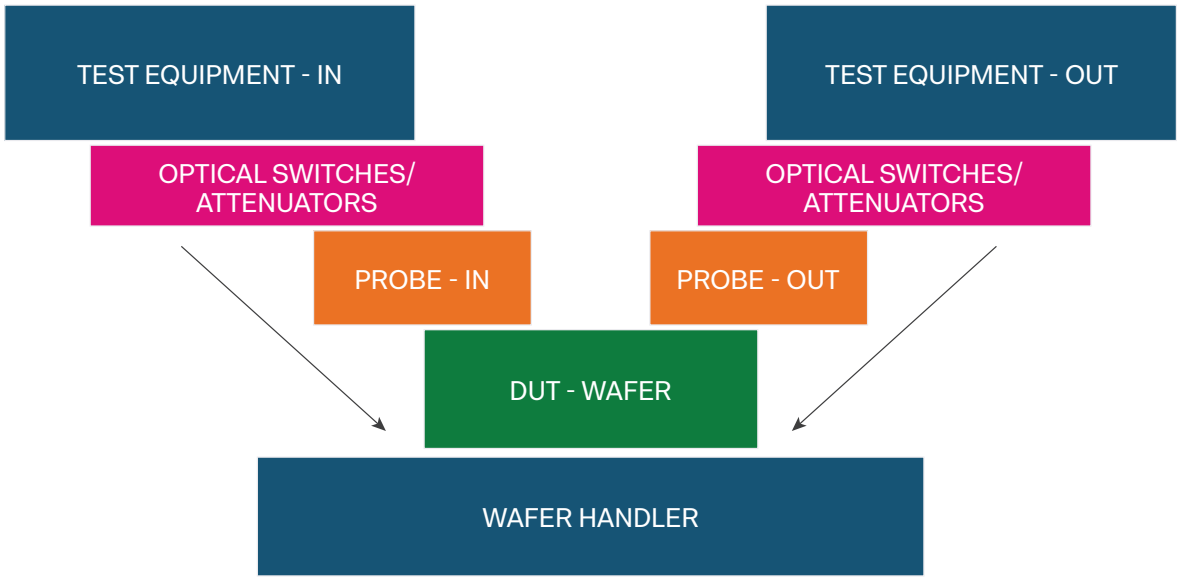
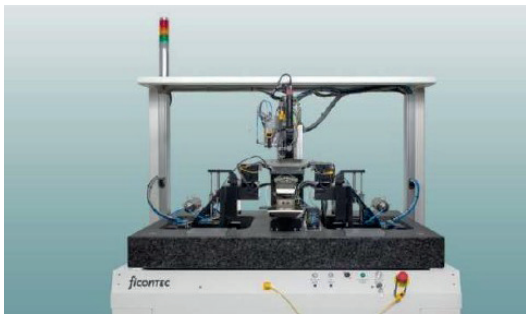


Figure 7: An example of a generic wafer probing and measurement set up.

An overview of the test functions Quantifi Photonics offers can be found on the Quantifi Photonics website[9].

Fiber Array Alignment & Assembly

One of the key challenges mentioned previously is the mass parallelization of next-generation optical interconnects, and consequently the need to perform cost-effective fiber array alignment as part of the assembly process. With dozens or hundreds of channels to test, speed and efficiency will be critical to ensure shipped products meet specification.



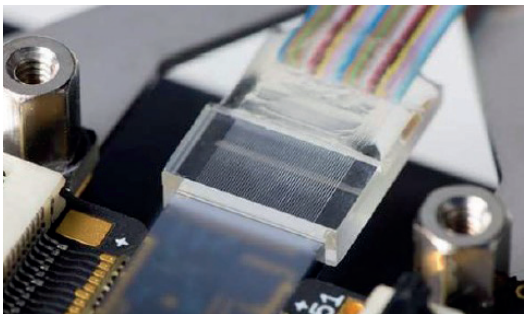


Image 13/14: Photonic assembly and alignment equipment (**Source:** ficonTEC).

A schematic of the setup that enables such testing follows (figure 8). The assembly equipment - such as ficonTEC's Photonic Device Assembly equipment[10] - positions the fiber array relative to the device-under-test and actively monitors the output levels from the array of photodetectors. This enables the optimum fiber array position while curing the adhesive between DUT and fiber array, as well as validating that all channels of the DUT are performing within spec. Assuming it passes, the optical subassembly can be progressed to the final stage of the manufacturing process, which is the assembly of the packaged product.

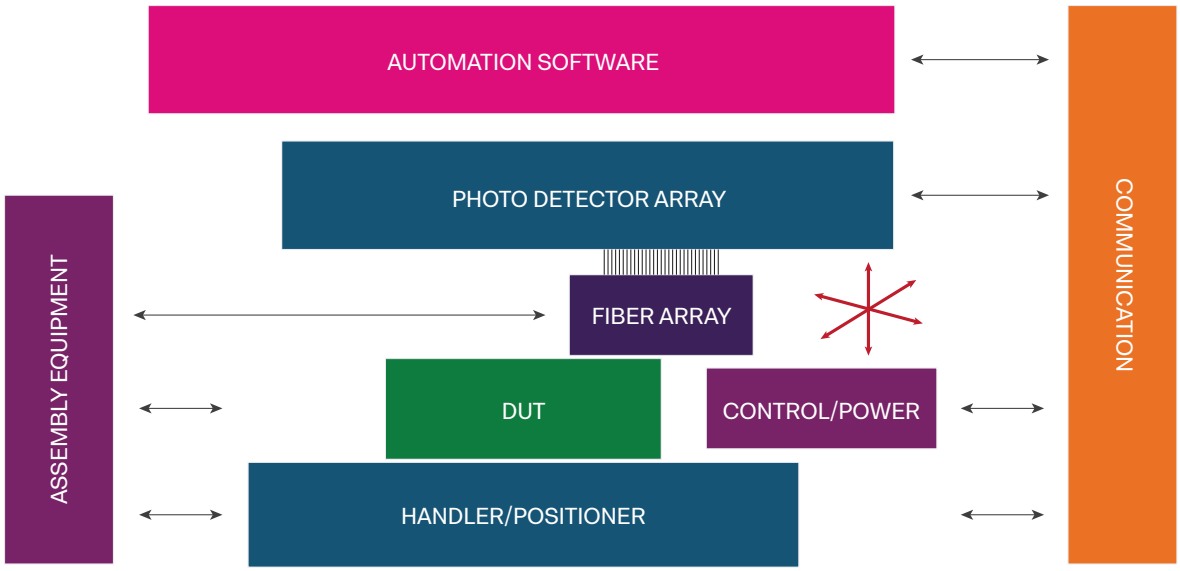


Figure 8: Block diagram of an example test setup for fiber array alignment and assembly.

Module Test At-Speed Optimization & Spec Compliance

This can be considered the final step in the manufacturing cycle. The product is fully assembled in its desired form factor such as OSFP-XD[11] or OIF 3.2T CPO module and is undergoing the last optimization step and pass/fail test before it ships to the customer. This setup typically includes a test fixture to support high-speed signal access to the optical module, and it may be subjected to thermal stress via a TEC cooling/heating element or a thermal stream.

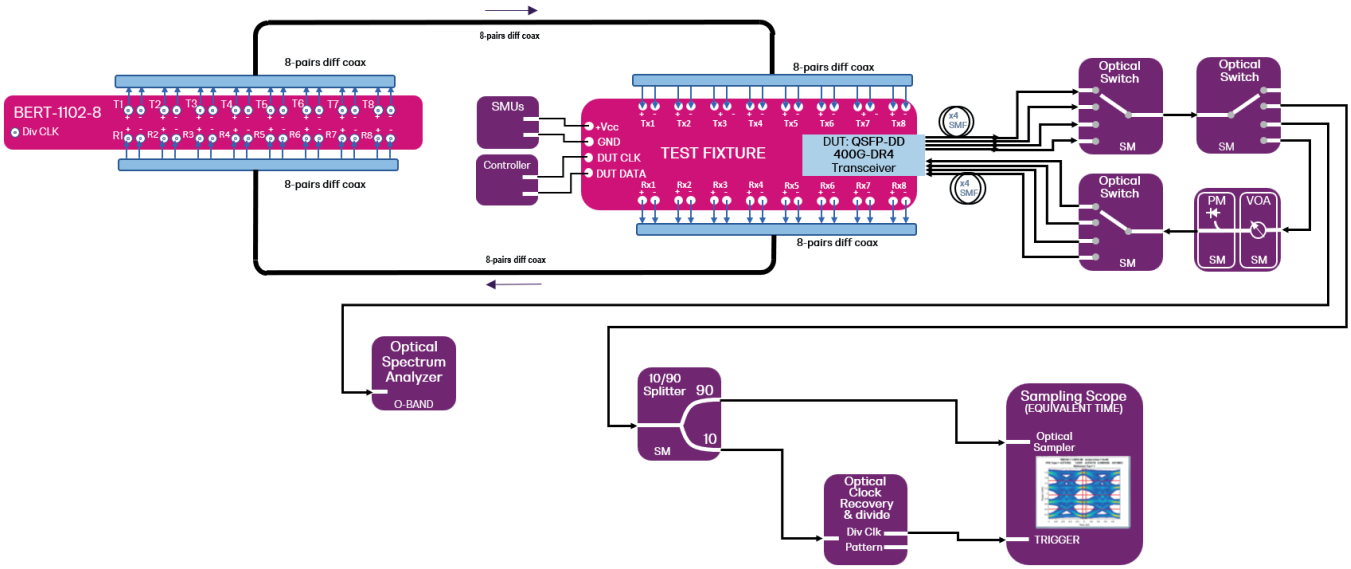


Figure 9: Block diagram of a test setup enabling characterization of the optical spectrum, at-speed testing of transmitter eye diagram, TDECQ, and receiver sensitivity.

The setup (figure 9) above enables characterization of the optical spectrum, and at-speed testing of transmitter eye diagram and TDECQ, as well as receiver sensitivity. This characterization allows the final tweaking of device parameters before it ships with maximum yield for spec compliance such as the 802.3 Ethernet spec 400GBASE-DR4[12].

Image 15: Key equipment for module test - thermal stream, MSA-compliant MCB, test instrumentation.

Test Evolution of Co-Packaged Optics Devices

This section discusses the testing evolution from a Silicon Photonics wafer through to a CPO module ready to be shipped to an end user and deployed in a hyperscale datacenter or AI/ML high-performance computer network.

There are four different stages in the product life cycle: R&D, validation and characterization, manufacturing, and deployment, each with their own specific test requirements. On top of this are the different manufacturing stages from wafer, die/PIC, assembly and alignment, to packaged product, that impact the test strategy as well. Initially the focus is to understand whether the design works and feedback test results to the design software for product optimization. Environmental stress testing needs to start as early as possible to understand the reliability and effective lifetime of the product, and to address potential risks early in the process. Full validation over process and operational corners as part of the ODVT (optical design verification testing) in the middle of the life cycle will help to minimize testing in later stages and improve the overall manufacturing cost structure. The developer will first perform a lot of this testing in close cooperation with its supply chain partners such as foundries, OSAT houses, and contract manufacturers. In later stages the supply chain partners will own most of this process for an optimized manufacturing and test flow. Typically in the earlier stages it is best to test all parameters to fully understand product and process, which then allows testing of a subset of critical parameters in volume manufacturing for reduced cost of test and optimized manufacturing flow.

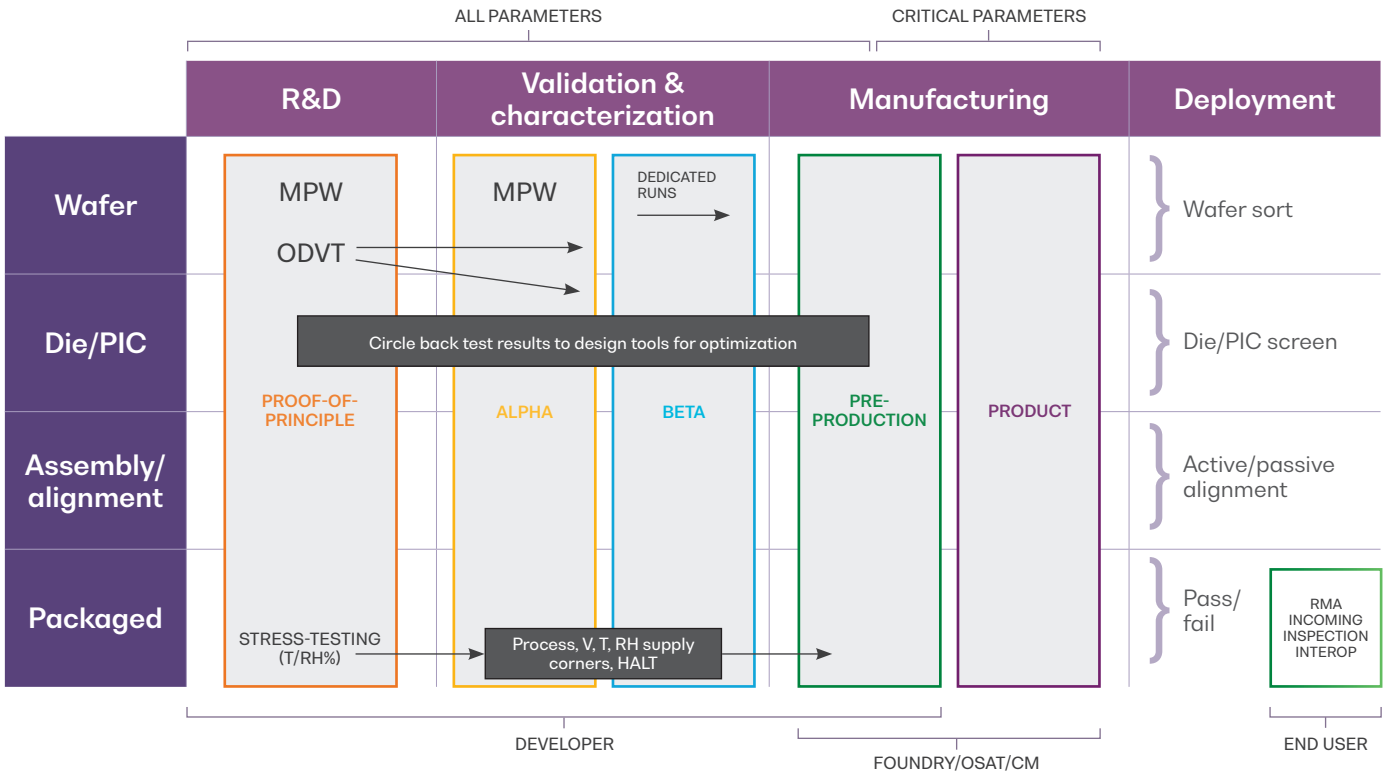


Figure 10: Co-Packaged Optics test evolution: overview.

CPO test examples

In the R&D phase it is important to gain insight into the performance of the critical elements and optimize if needed. For instance, testing the design of ring resonators to optimize the coupling coefficient, filter bandwidth, decrease crosstalk and achieve desired channel separation.

Another critical element to test early in the process is the modulation depth and bandwidth of the high-speed modulator. These elements determine whether this implementation is going to provide the proper wavelength demultiplexing and high-speed I/O function.

To support the PIC manufacturing cycle, studying die performance variations across the wafer will identify screening parameters that can be applied in manufacturing to maintain performance expectations (screening vs by design). Initially a lot of data is gathered to understand what qualifies as a good wafer and a good die. These insights can be applied so that later in the process, more simple screening parameters will be sufficient to determine good wafers and dies. Additionally, a wafer burn-in procedure will help weed out infant mortality and guarantee the lifespan of the product.

Since in most cases the polarization of the incoming light cannot be controlled the validation of polarization dependence needs to yield satisfactory results, as well as the validation that the PIC can operate over the specified wavelength range. Tunable lasers and optical spectrum analyzers, polarization controllers and photodetectors, are typical instruments that enable this. For instance, the validation of the laser source needs to ensure that wavelength, linewidth, power, and side mode suppression all meet the specifications over process, voltage and temperature corner cases.

Beyond testing the high-speed interfaces, packaged devices should be subjected to link and system tests to make sure these devices can properly interoperate in the system environment they are designed for. Environmental stress testing and highly accelerated life testing including exposure to high humidity and temperature will demonstrate that these densely integrated products are reliable and can provide significant data throughput in a network environment with an acceptable mean-time-between-failure (MTBF). Since CPO devices typically carry multiple terabits per second of data traffic the proven reliability of these devices is becoming more important than ever compared to the smaller and easier to replace pluggable optics.

Fully understanding device behavior by testing all channels is important in many stages of the life cycle and this needs to be planned accordingly. Especially in manufacturing, having the ability to test dozens or hundreds of channels efficiently will help provide the cost-effective test flows and manufacturing output that are needed to make CPO commercially attractive.

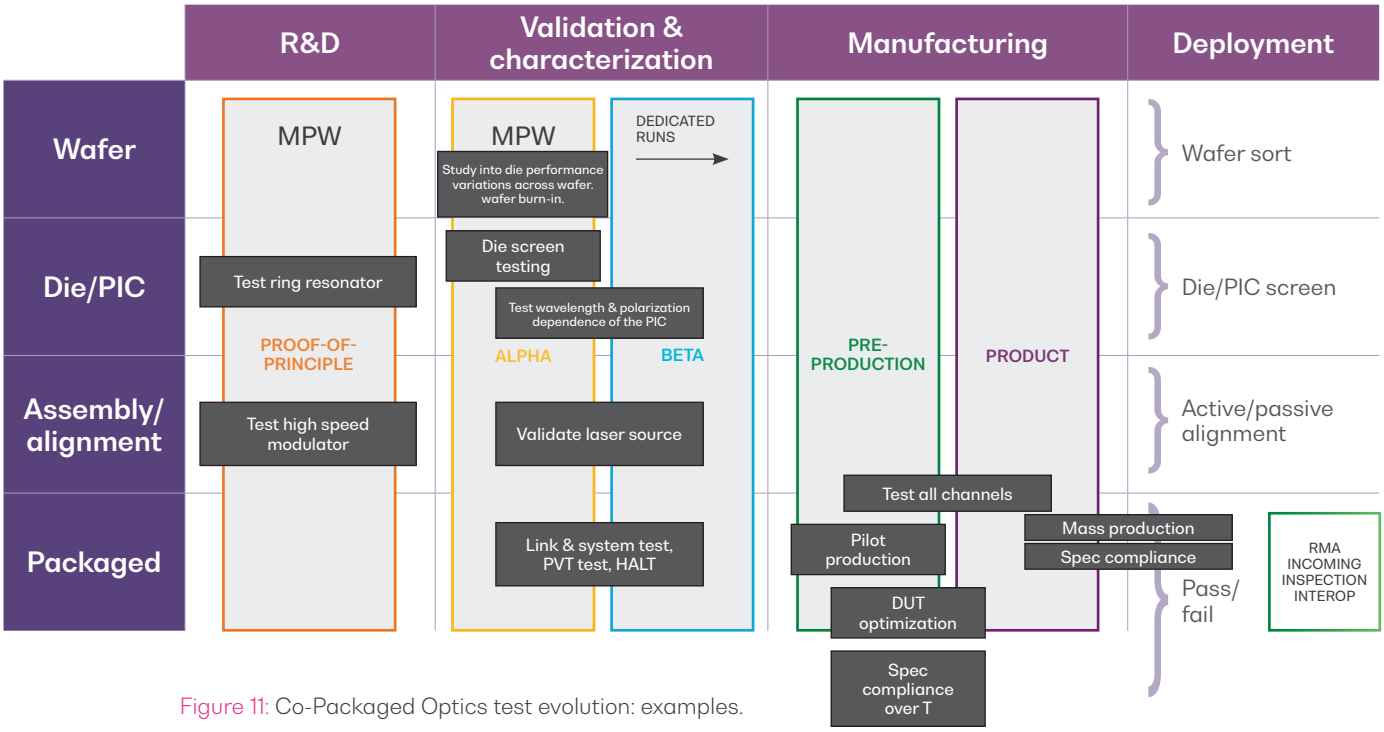


Figure 11: Co-Packaged Optics test evolution: examples.

In pilot manufacturing even more data needs to be processed to optimize the product and validate that the product meets specifications. It is likely that a temperature screen is part of this initial manufacturing test. Once there is satisfactory correlation and understanding of screening parameters, a less complex test regimen can be applied in mass production and still produce in-spec CPO devices with even greater throughput.

In the deployment phase, testing requirements change yet again. Ideally, operator-friendly test solutions can provide incoming inspection tests or conclusive RMA analysis with the single click of a button, and output a detailed test report indicating pass/fail test results relative to the applicable standard specification.

Conclusion

The CPO Test Life Cycle is complex and varies from production of the first wafer to final product being shipped to the customer. In **R&D**, maximum flexibility is required and a mix of benchtop test instruments that can change on the fly is preferable. In **validation and characterization**, when lots of test data needs to be acquired, and processed, proper planning of more densely integrated test benches that can easily be automated and integrated into wafer handling probe systems and advanced manufacturing and alignment equipment may provide maximum downstream benefits. The test bench needs to be flexible as test requirements will evolve over time.

In **manufacturing**, test requirements have converged into the final product manufacturing test bench. The most densely integrated test solution that can provide the parallel characterization of CPO test modules with hundreds of channels, in combination with another densely integrated test bench that includes basic functions such as SMUs and OSAs, will provide the cost-effective test environment that can produce large volumes of high-quality CPO modules in a commercially attractive manner.

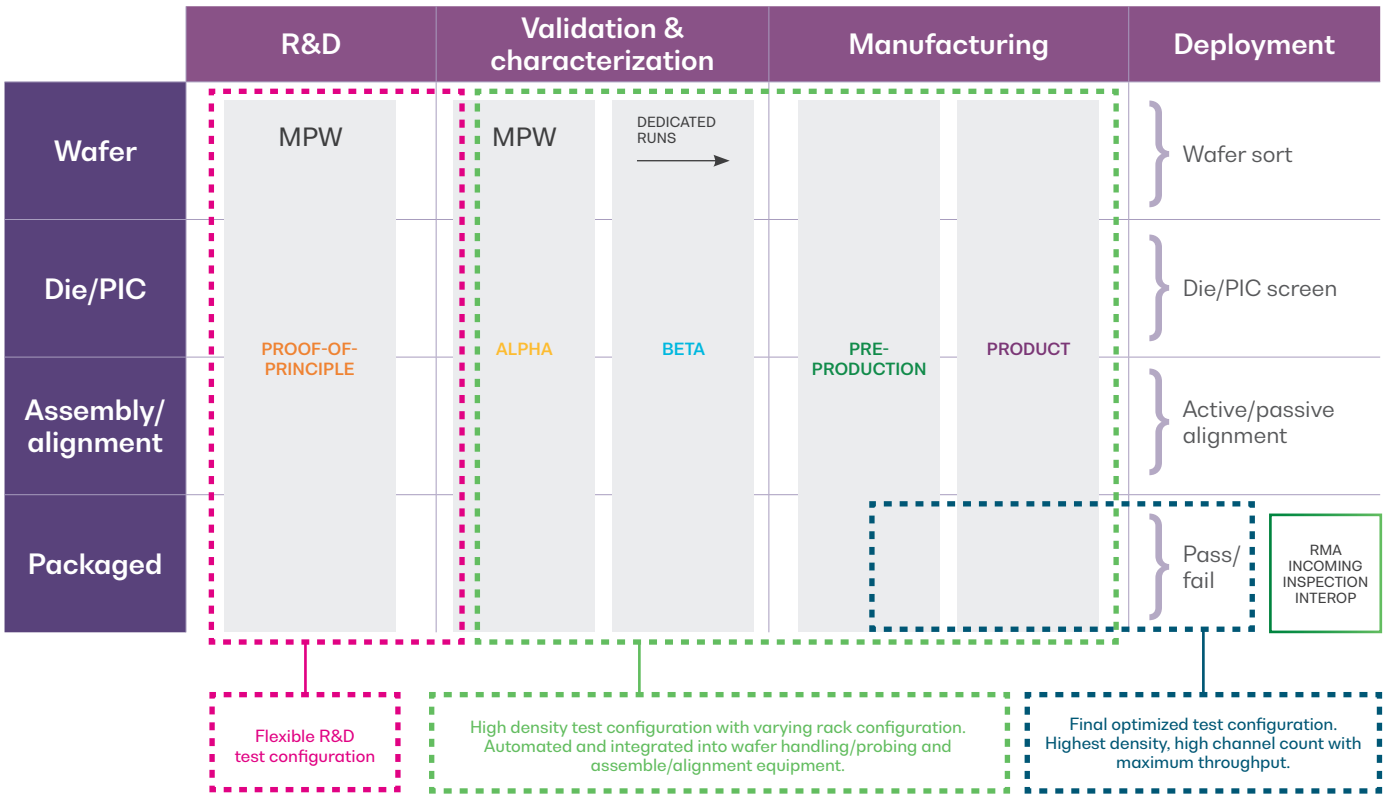


Figure 12: Co-Packaged Optics test evolution: summary.

Cost-of-Test

The actual cost-of-test, described as dollar cost per unit tested, depends heavily on the specific details of the chosen manufacturing and testing strategy and there is no golden formula that can be applied in all cases. However, this section will discuss some of the critical elements to pay attention to. In particular, the cost-of-test as part of the manufacturing cycle is highlighted since this directly impacts the cost-of-goods-sold (COGS) of the optics.

Capital Expenditures (CapEx)

The initial outlay of funds is always top of mind, however this may not be the most important factor. It is of course cost prohibitive to pay for premium equipment designed for advanced R&D and to use it in manufacturing. It is much more preferable to pay for the exact features, capabilities and quality that is required for the manufacturing test. In addition, capital expenditures can be amortized over the effective lifespan of the product, and it may be prudent to identify the cost determining factors that have a more direct influence on the cost-per-unit.

Operational Expenditures (OpEx)

The expenditures that directly impact the cost-per-unit are the variable cost of all the activities related to producing the units and includes the human resources to load equipment and actually manufacture the product. Photonics assembly equipment as mentioned earlier optimizes this part of the equation and is therefore a critical element in the manufacturing cycle. In addition, there are other factors impacting OpEx listed below.

Image 16: Automated photonics assembly equipment. (**Source:** ficonTEC).

Test Time

The time it takes to test a device directly impacts the resource consumption (and therefore cost), and it should be optimized to be a small fraction of the overall process. There is setup time, optimization of the probes, heating or cooling the DUT, and ongoing system maintenance, etc. Then once the DUT is ready, the test time should be quick relative to those other steps. A few minutes per test is typically undesirable, but a few seconds (or at most tens of seconds) for complex tests, and a fraction of a second (or at most seconds) for the more mundane test tasks are reasonable targets. For a wafer screen where multiple hundreds or thousands of dies are tested sequentially the test time per die is paramount to minimize overall test time.

Parallelization

To further optimize resource utilization, test engineers should aim to maximize the number of channels and/or number of devices tested at the same time. Ideally, this will increase test throughput and lower the operating expenditures. Parallelization is all about using the testing and assembly infrastructure efficiently which may require slightly higher initial CapEx but over time, cost-of-test will track lower.

Test Flow Optimization

It is critical to optimize the overall test flow to further lower the cost of test, which admittedly may be more of an art than science and come from years of hard-won experience. Optimizing what is to be tested and in which sequence can reduce overall test times and deserves special attention.

Space

Rack and floor space is always limited due to its high cost (rent or other real estate expenses), and is an important consideration. Fitting lots of test instrumentation in densely populated racks has a significant cost advantage so instrument footprint and overall channel and system densification should not be overlooked.

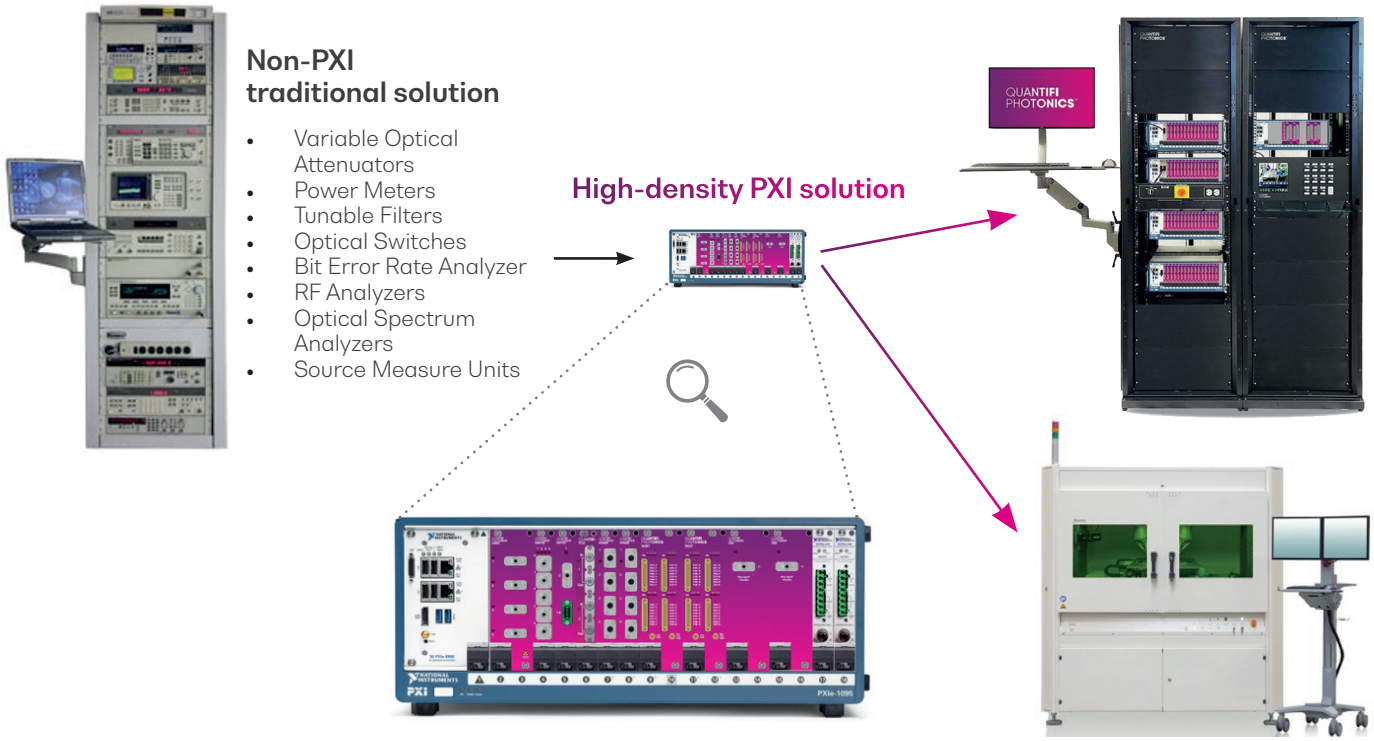


Figure 13: A comparison of the size of traditional test instrumentation compared to a PXI-based equivalent.

Solutions

Test Functions

To address all the requirements outlined previously, Quantifi Photonics suggests the following broad spectrum of test functions to be part of the standard optical or photonics test bench:

Fixed laser

Provide a precisely controlled specific optical wavelength signal.

Optical to electrical converter

Bring the optical signal into the electrical domain for further analysis.

Tunable/swept laser

Step or sweep through the wavelengths of interest.

Optical spectrum analyzer

Analyze the optical power as a function of wavelength.

Broadband light source

Provide full spectrum of light simultaneously.

Bit error rate tester (BERT)

High-speed pattern generator and error detector.

Polarization controller & scrambler

Control the polarization of light accurately or sweep through all polarization states of interest.

Optical switch

Route the optical signal to a selectable output for automated testing.

Optical power meter

Measure the optical power to determine insertion loss or optimize alignment.

Variable optical attenuator (VOA)

Precisely control the optical power level.

Traditional PXI modules

Add other PXI modules such as an NI Source Measurement Unit.

Benchtop instruments

Tektronix Optical Clock Recovery and Sampling Oscilloscope.

Form Factor

In addition, Quantifi Photonics proposes three form factors to support the testing requirements outlined previously. The key is to support the flexible test bench with a varying range of test functions, from R&D to manufacturing and deployment, and to provide the optimum (and customized if needed) optical test bench in volume production. This can all be easily integrated into assembly and manufacturing equipment systems to handle and manufacture the wafers, dies, and ultimately pluggable or other modules.

Industry standard high-density rack-mountable test modules - PXI

PXIe: the standardized rack mountable instrument form factor, which enables high density test benches with a flexible variety of test instruments.

The power of the PXI platform cannot be underestimated. It enables a flexible, high-density test bench with a wide variety of test modules, from SMUs to digital acquisition cards for a broad range of industries and applications. The PXI modules have standardized interfaces facilitating the creation of complex test benches for the end user's specific needs. PXI enables synchronized triggers to be able to create fast and optimized test flows across multiple test instruments. PXI is ideal for complex test setups in volume test applications such as validation and manufacturing where lots of devices need to be tested with potentially multiple setups. In these applications density and scalability is paramount to be able to test a high volume of products in a relatively small footprint.

Flexible bench top test instruments - MATRIQ™

MATRIQ: small bench top instrument for flexible R&D, easily mix and match instruments on the test bench.

Custom maximum density 19 inch rack mountable test modules - EPIQ™

EPIQ: the solution with maximum instrument and channel density, as well as the ability to act as a custom platform for the final test configuration in manufacturing with the highest density and cost effectiveness.

Use Case: ficonTEC Service GmbH; Integrating Test Processes into Manufacturing Capability

T&M processes for die-level integration and manufacturing have long been a critical aspect of ficonTEC's production systems. More recently it became obvious at ficonTEC that T&M needs its own space, and much more focus has gone into this area as a consequence. By drawing on both internationally funded R&D collaborations and innovation with industrial partners, ficonTEC is working to evolve and optimize T&M capability for various stages of a photonic device high-volume manufacturing process.

R&D & Production T&M Capability

For early wafer-level test, for example to determine non-singulated device yield across a wafer, flexible electro-optical (e/o) wafer test systems are already available to test optical element I/O and more complex PIC devices individually and sequentially. For specific use cases, this capability has also been extended to testing of multiple devices in parallel, thus optimizing the efficiency of the test process at each dwell point of the motion system across the wafer.

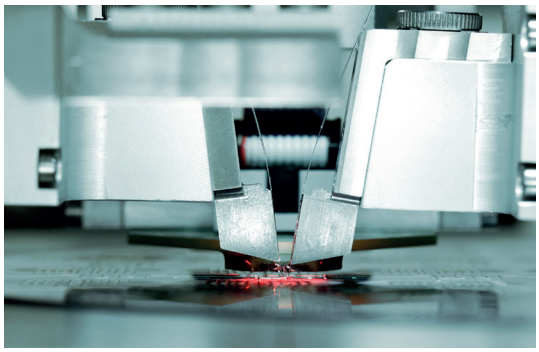


Image 17: Combined e/o wafer-level test (**Source**: ficonTEC).

By automating device characterization and verification in tandem with traceability, vital efficiency and reliability is added to the determination of wafer yield and performance across entire wafers, resulting in extremely valuable and previously unattainable feedback for the wafer fabs. A re-configurable e/o probe layout even caters to multiple PIC designs on a multi-project wafer (MPW).

At the point where a wafer becomes divided into smaller device groups or even individual dies, this type of system easily adapts to custom (carrier) formats. Irrespective of the format, for volume manufacturing identical devices can be tested fully automatically, either individually or in parallel.

At any of these stages, one important design consideration is the approach for coupling light into and out of the device under test (DUT). Grating couplers are a well-accepted approach, coupling light diffractively into or out of the DUT in question. Alternatively, custom 3D-printed fiber tips provide support for low-loss edge-coupling via 50 nm trenches designed into the wafer surface at the point of optical I/O.

Moving along the production process, versatile e/o test systems are available to test more complicated opto-electronic

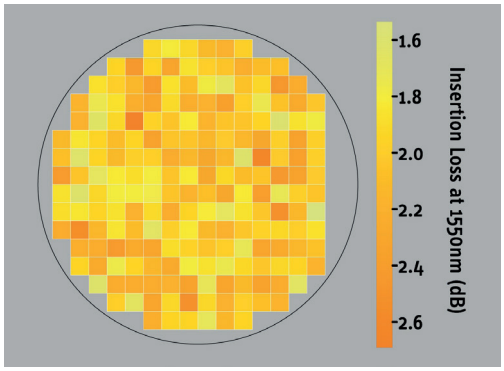


Image 18: Waveguide test across an entire PIC wafer, with performance/yield cataloging (**Source**: VLC Photonics).

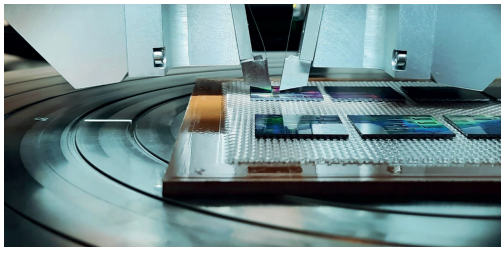


Image 19: Optical dual fiber I/O for custom carrier formats. (**Source**: VLC Photonics).

components and PIC-based sub-assemblies. Other complex tasks include LIV, spectral, polarization and near/far-field beam characterization of single laser chips (incl. VCSELs), unmounted laser diode bars and chip-on-submount (CoS) sources. These die-level systems can also be routinely equipped to perform detailed optical facet inspection using Deep Learning for defect recognition.

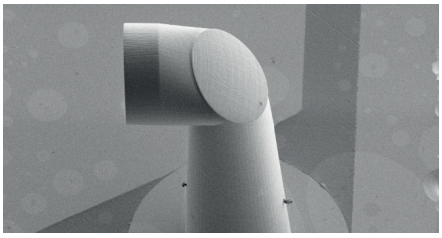


Image 20: 3D printed periscope on the end of an optical fiber, as used for edge coupling (**Source:** ficonTEC).

In order to keep all stages of the overall production process 'high volume', individual wafer, die and device-level assembly and test processes can be assigned to task-specific in-line systems, where optimized sequencing and orchestration of these systems establishes a fully operational production line. Wafers, dies or devices can thus be tested, verified and remain traceable at all designated points along the production process.

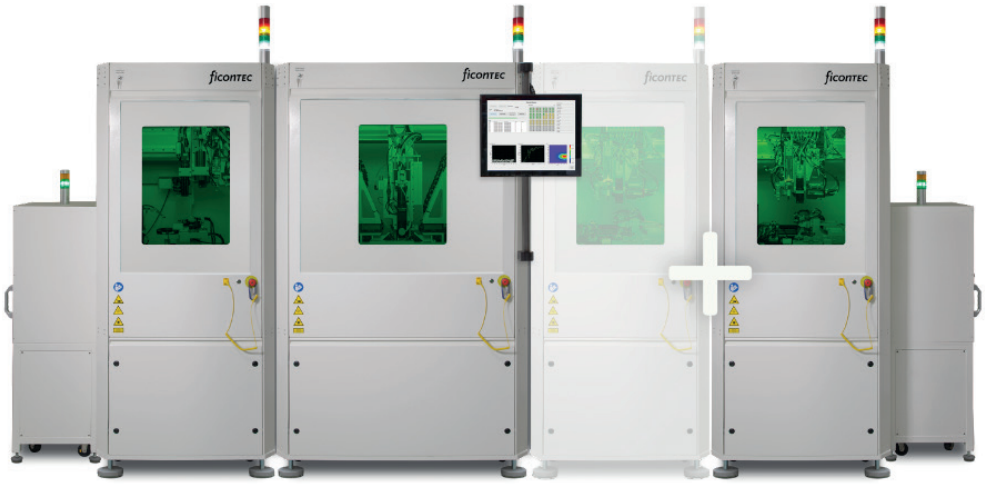


Image 21: ficonTEC custom in-line assembly & test machine sequencing.

Requirements for T&M Instrumentation

In order to meet the future challenges for reduction in cost-of-test as well as the time constraints imposed by the throughput requirements implied by the market forecasts, the future of photonic device testing will require further advanced automation in tandem with the implementation of parallel T&M processes.

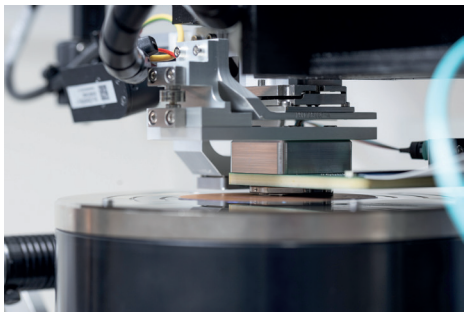


Image 22: Multiple device e/o test head over VCSEL wafer (**Source**: ficonTEC)

At wafer level, even fast active optical I/O alignment currently forms the bulk of the time budget across a high-density device wafer, so the ultimate goal is to develop massively parallel e/o I/O T&M heads capable of addressing multiple devices per alignment process. Such T&M heads can of course be wafer specific. Or, alternatively, given sufficient device standardization, wafer-savvy motion systems – motion algorithms that maximize throughput for a T&M head capable of parallel measurement of x by y devices over a wafer of X by Y total devices for the available throughput of the T&M instrumentation.

Greater parallelization is not the only route to increased T&M complexity. For example, in a scenario where real-time device correction is possible to bring up wafer yield early in the production process, T&M head complexity further increases as does the need for correction process control instrumentation.

It then becomes clear that a lack of throughput (multiplicity or multiplexing) capability of the T&M instrumentation set-up forms a major bottleneck. High density and/or rapid switching of what will likely be high-channel-count instrumentation then becomes a critical aspect of the overall throughput calculation.

Following singulation and continued assembly later in the production process, device and package complexity and the associated T&M scenarios change appropriately. Indeed, the development of high-channel-count optical interconnects as discussed in the introduction of this white paper testify to the increasing T&M demands presented by current integrated photonic package evolution.

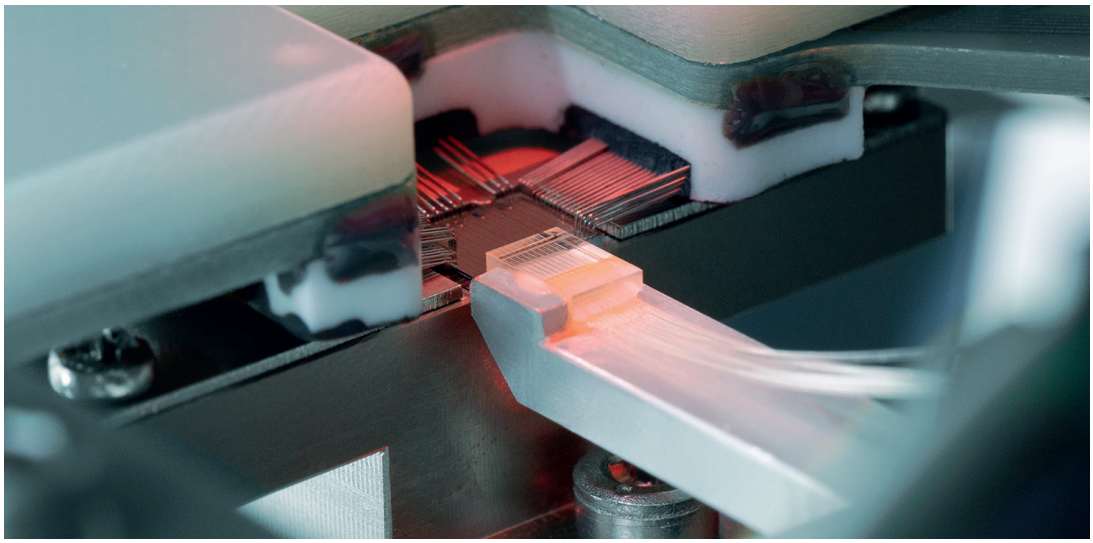


Image 23: High-channel count die-level test (**Source**: ficonTEC).

PXI Integration

ficonTEC assembly & test production systems already feature their own unified process-oriented control interface that ships with all turn-key stand-alone systems and multiple machine configurations. This interface allows individual process programming and automatically orchestrates all movement, wafer/die/device handling, assembly and T&M scenarios, and optimizing the production process for any specific need.

This interface is already compatible with Quantifi Photonics' PXI-based instrumentation architecture – seamlessly via API utilization. Sophisticated e/o test solutions have already been realized to match customer-specific requirements, and can be rapidly modified to suite evolving needs.

Conclusions

The future of data center infrastructure and high-performance computing is going to rely even more on optical interconnects as copper is running out of steam at 100 Gbps per channel and beyond.

Silicon Photonics and Photonic Integrated Circuits are key enabling technologies and require a new approach as wafers and dies need to be tested optically as part of the manufacturing process.

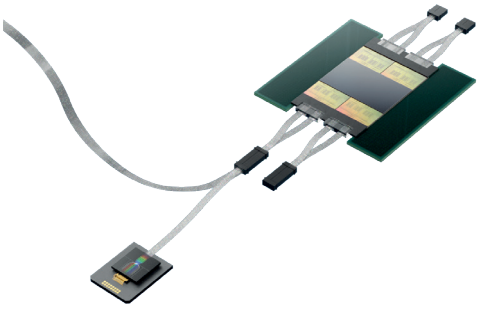


Image 24: Ayar Labs SuperNova™ light source and TeraPHY™ optical I/O chiplet.

Densification and mass parallelization of optical interconnects, through co-packaged optics and in-package optics, is on the horizon due to the drive to reduce power in data centers, and to remove compute bottlenecks for the enablement of next-generation ML/AI/HPC computer networks.

The combined effects of these trends are driving the industry to adapt. Participants are looking for ways to copy the mature semi-conductor ecosystem where development, manufacturing and testing are all nicely integrated from design tools, IP creation, to foundries, test and assembly houses, and contract manufacturing.

Quantifi Photonics proposes a testing infrastructure with the following characteristics that can lay the foundation of the test methodology for this new Integrated Photonics ecosystem. In addition, Quantifi Photonics is partnering with leading developers of next-generation optical interconnects as well as equipment manufacturers and service providers to help move the industry forward.

- **Flexible:** choose from a wide selection of test modules in a variety of form factors, and vary the mix as the testing needs evolve
- **Scalable:** increase test system channel count from a few channels to multi-DUT, multi-port testing with hundreds of channels
- **High-Density:** the field-proven PXI test platform can support up to 17 single width test modules in a single 4 U high, 19-inch test rack. Custom test configurations can be designed into an even higher density form factor.
- **True Mixed-Signal:** both optical and electrical testing in a cohesive platform
- **Versatile:** wide selection of optical and electrical test functions that can be used to build a complete optical test bench
- **Ease of integration:** test instruments with a common GUI and API, and can be easily integrated into a system with assembly and other equipment

Image 25: Quantifi Photonics PXIe-based test instruments.

Acknowledgements

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